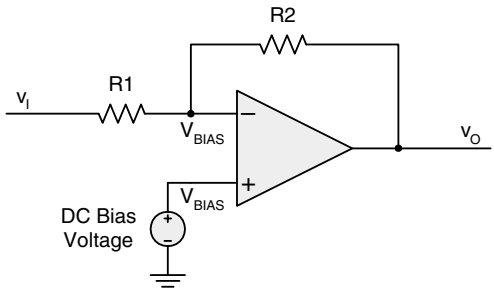

FIGURE 14.6 Biased inverting op-amp circuit.

pensate for, V_{BIAS} = 2.4 V ÷ 1.8 = 1.33 V. The specific bias voltage required may not be readily available. In these circumstances, a voltage divider may be employed at the positive input to produce an arbitrary bias voltage from a common supply such as +5 or +3.3 V. This scheme enables an op-amp to be used in the inverting configuration with a single supply voltage as long as the bias voltage is sufficient to produce a minimum output voltage of zero.

14.2 CHARACTERISTICS OF REAL OP-AMPS

Real op-amps are subject to the same laws of physics that cause nonideal behavior in all types of devices. The degree to which these deviations negatively affect a system varies according to the specific circuit. Op-amp manufacturers provide detailed data sheets to accompany their products, because many parameters must be characterized to enable proper circuit design. Fairchild Semiconductor's venerable LM741 serves as a useful example with which to explore real op-amp specifications. A portion of the LM741 data sheet is shown in Fig. 14.7.

Nonideal input characteristics are specified in the top portion of the LM741's data sheet. *Input offset voltage*, V_{IO}, is a DC error introduced by the op-amp's internal circuitry that manifests itself as an applied differential voltage between the two inputs. Assuming an ideal op-amp, V_{IO} appears as a voltage source applied by the external circuitry. If 0 V is applied to the op-amp, the input voltage is actually equivalent to V_{IO}. If a real op-amp is powered on in an open-loop configuration, its very large, though not infinite, open-loop gain can cause the output voltage to saturate because of the nonzero input voltage due to V_{IO}. The LM741's open-loop gain, shown as G_V in the data sheet, is between 20 and 200 V/mV. With V_{IO} = 2 mV, the output voltage is forced to its limit. Of course, op-amps are not generally used in an open-loop configuration. Figure 14.8 shows a common op-amp configuration in which the circuit's two inputs are grounded. The inputs are grounded to simplify analysis of V_{IO} effects in the absence of an input signal. When an input signal is present, the V_{IO} effects are added to the input/output transfer function. V_{IO} is represented as a separate voltage source applied to an ideal op-amp. Because V_{IO} appears as a differential voltage, the op-amp's output is approximated by the idealized closed-loop noninverting gain relationship: $V_O = V_{IO}$ (1 + R2 ÷ R1). This is essentially the same situation as the biased inverting op-amp circuit shown in Fig. 14.6, although the bias voltage is undesired. Therefore, the input offset voltage is amplified along with signals that are applied to the circuit.

It can be difficult to compensate for input offset voltage, because each individual op-amp has a different polarity and magnitude of V_{IO}, making it impossible to design a circuit with a fixed compensation factor suitable for all devices. Additionally, V_{IO} changes with temperature. Depending on

Electrical Characteristics

(V_{CC} = 15V, V_{EE} = - 15V. T_A = 25 °C, unless otherwise specified)

Parameter		Symbol	Conditions		LM741C/LM741I			Unit
					Min.	Typ.	Max.	
Input Offset Voltage		V_{IO}	$R_S \leq 10K\Omega$		-	2.0	6.0	mV
			$R_S \leq 50\Omega$		-	-	-	
Input Offset Voltage Adjustment Range		$V_{IO(R)}$	V_{CC} = ±20V		-	±15	-	mV
Input Offset Current		I_{IO}	-		-	20	200	nA
Input Bias Current		I_{BIAS}	-		-	80	500	nA
Input Resistance (Note1)		R_I	V_{CC} =±20V		0.3	2.0	-	MΩ
Input Voltage Range		$V_{I(R)}$	-		±12	±13	-	V
Large Signal Voltage Gain		G_V	$R_L \geq 2K\Omega$	V_{CC} =±20V, $V_{O(P-P)}$ =±15V	-	-	-	V/mV
				V_{CC} =±15V, $V_{O(P-P)}$ =±10V	20	200	-	
Output Short Circuit Current		I_{SC}	-		-	25	-	mA
Output Voltage Swing		$V_{O(P-P)}$	V_{CC} = ±20V	$R_L \geq 10K\Omega$	-	-	-	V
				$R_L \geq 2K\Omega$	-	-	-	
			V_{CC} = ±15V	$R_L \geq 10K\Omega$	±12	±14	-	
				$R_L \geq 2K\Omega$	±10	±13	-	
Common Mode Rejection Ratio		CMRR	$R_S \leq 10K\Omega$, V_{CM} = ±12V		70	90	-	dB
			$R_S \leq 50\Omega$, V_{CM} = ±12V		-	-	-	
Power Supply Rejection Ratio		PSRR	V_{CC} = ±15V to V_{CC} = ±15V $R_S \leq 50\Omega$		-	-	-	dB
			V_{CC} = ±15V to V_{CC} = ±15V $R_S \leq 10K\Omega$		77	96	-	
Transient Response	Rise Time	T_R	Unity Gain		-	0.3	-	μs
	Overshoot	OS			-	10	-	%
Bandwidth		BW	-		-	-	-	MHz
Slew Rate		SR	Unity Gain		-	0.5	-	V/μs
Supply Current		I_{CC}	$R_L = \infty\Omega$		-	1.5	2.8	mA
Power Consumption		P_C	V_{CC} = ±20V		-	-	-	mW
			V_{CC} = ±15V		-	50	85	

Note:
1. Guaranteed by design.

FIGURE 14.7 LM741 data sheet. *(Reprinted with permission from Fairchild Semiconductor and National Semiconductor.)*